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Partners from RF to Light

GaN-on-Silicon for 5G Radios

Timothy Boles – MACOM Technology Solutions

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Bringing together the entire microelectronics supply chain™

Agenda

- Introduction to 5G
  - Why 5G
  - 3G to 4G to 5G Transition
  - Frequencies – Microwave & mmW
- Impact on Device Technologies
  - 4G Imcumbent - LDMOS/GaN
  - 5G Future – GaN/GaAs/Silicon CMOS/SiGe & Massive MIMO Implications
  - RF System Operating Voltage & Technology Impact
- GaN Revolution for 5G
  - Market vs Price
  - GaN-on-Silicon vs GaN-on SiC
  - Supply Chain
- Future Expectations/Possibilities

Introduction to 5G

3G -> 4G -> 5G Transistions

Why 5G

- Faster Data Rates
- Internet Connectivity
- Lower Latency
- Video
- Robotics
- Automotive
- Medical/Emergency Services
- All Require Substantial Increase in Bandwidth => Higher Frequencies

3G/4G Technology Trends

- 3G/4G Systems
  - Silicon LDMOS has been Incumbent Technology
  - Historical Operating Voltage – 50 volts
  - GaN has been Eroding Market Share Since 2015
- 4G Dominated by Macro Base Stations
  - Internally Matched Transistors in a Doherty Configuration
  - Operating Voltage – 50 volts Minimum
  - Final Stage Power Levels: 000's of Watts
  - Majority of applications 2.6 GHz and below
  - Very High Volume LDMOS Bands: 900MHz / 1800 MHz
  - GaN Making Significant Market Penetration

5G Technology Trends

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- 5G Sub–6GHz
  - Initial Roll-Out - Higher Frequency Version of 4G
  - Device Requirement - Tens to Hundreds of Watts
  - 3.5 GHz – 4.9 GHz Bands Will be Populated First
  - Antenna Technology – Massive MIMO Arrays
  - Longer Term – mmW Bands – 28 GHz, 39 GHz, 60 GHz
  - Operating Voltage – Function of Frequency - 50 volts -> 40 volts -> 28 volts
  - Maximize Overall System Efficiency
  - LMOS Cannot Meet Frequency Response at >24 volts
  - GaAs – Limited to ≈10 volt Operation
  - GaN is the ONLY Device Technology Choice

5G Technology Trends

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- 5G Moving to MIMO Antenna Configurations (from 2x2 to 8x8 and bigger)
  - Looks/Functions like a Phased Array Radar
  - Higher Frequencies/More Bandwidth
  - Power levels are dropping: P_{avg} ~ 5-10W – P_{peak} ~ 40 – 50W
  - Multistage Device (“MMIC”) – Integrated Driver and Final Stage
  - Approaches: (1) True MMIC, (2) MMIC + Output IPD, (3) Hybrid Construction
  - Output Stage is still Doherty configuration
  - Packaging: QFN and Laminate
  - MMIC Volume and TAM ($) will exceed Discrete Transistors significantly

mmW 5G Systems - MMICs

> mmW

- 28 GHz/39 GHz (Ka Band)
  - Multi-Beam Phase Shift Base Station Sites – MIMO/Pico Cells
  - System Efficiency => Higher Operating Voltages
  - PA Output Power Significantly Reduced – Few Watts
  - MMICs
  - Lower Voltage – 15 volts-28 volts? – Increase f_T
  - SAT Comm/DBS Adjunctcicy Issue
  - Open Frequency Allocations
  - LDMOS Eliminated at these Frequencies
  - GaAs Possible Competitor – Requires Significant Voltage Reduction
- 60 GHz (V Band)
  - Multi-Beam Phase Shift Base Station Sites – MIMO
  - PA Output Power Significantly Reduced – << 1 Watt
  - Low Operating Voltage
  - Open Frequency Allocation
  - SiGe/BiCMOS MMICs
  - Integrate Control Circuitry

A Transistor Market or MMIC Market?

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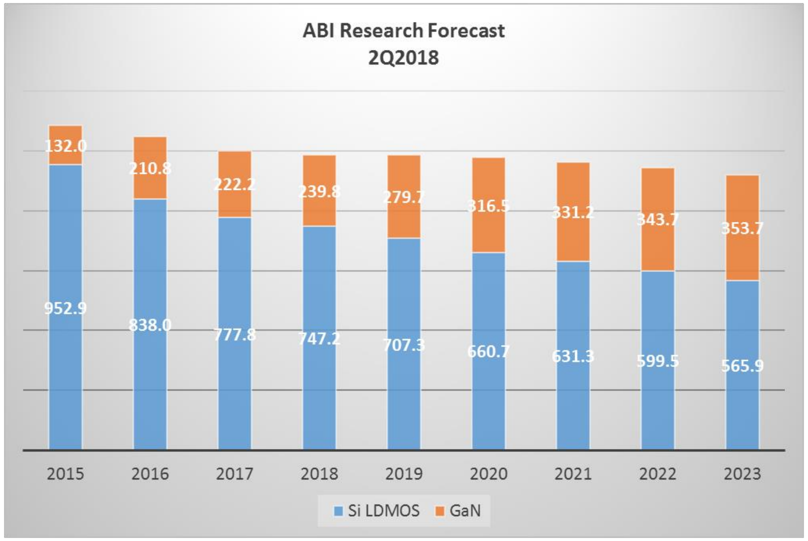

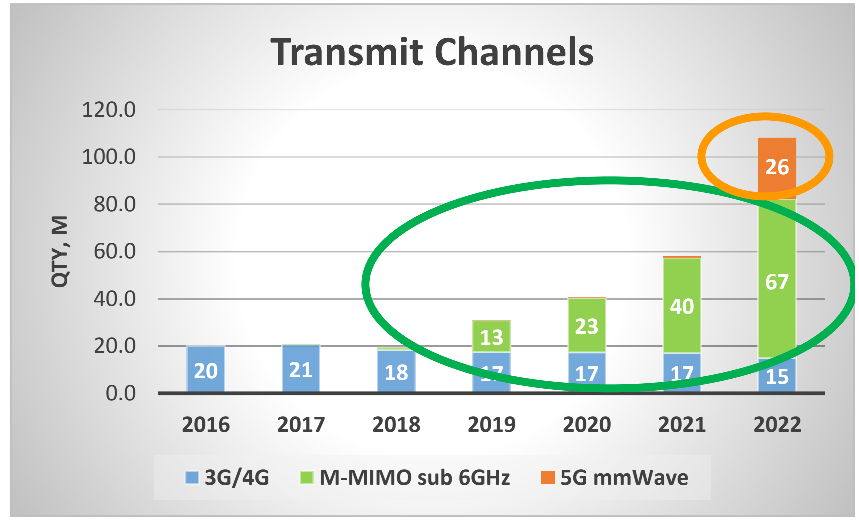

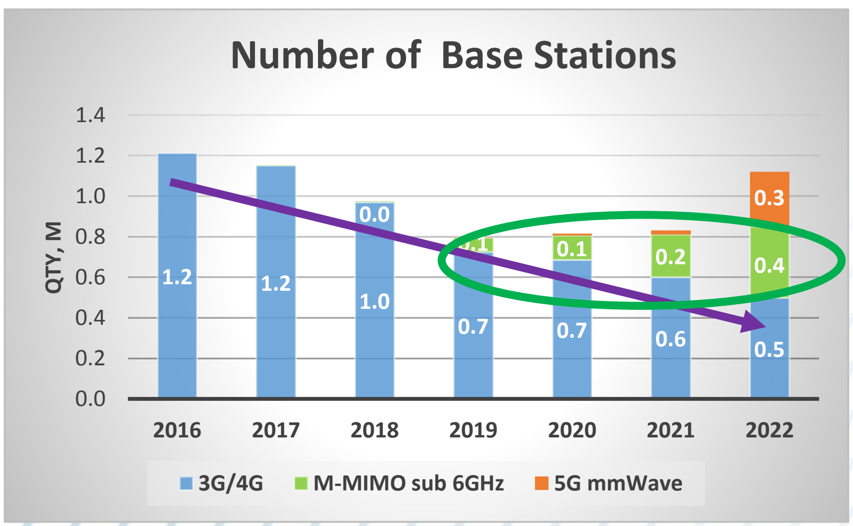

- GaN based devices will continue to grow taking market share from LDMOS
- Device volume growth will be in "MMIC's" both for sub-6 GHz and mmW
  - PA can be just a sub-component of TRx FEM
- # of Basestation is flat – BUT - device quantity increases – m-MIMO Arrays drive quantity
  - Device technology must support shift in antenna architecture

FY17 MACOM Estimates

Massive MIMO Implications

Why MMICs
MIMO Planar Antenna Arrays

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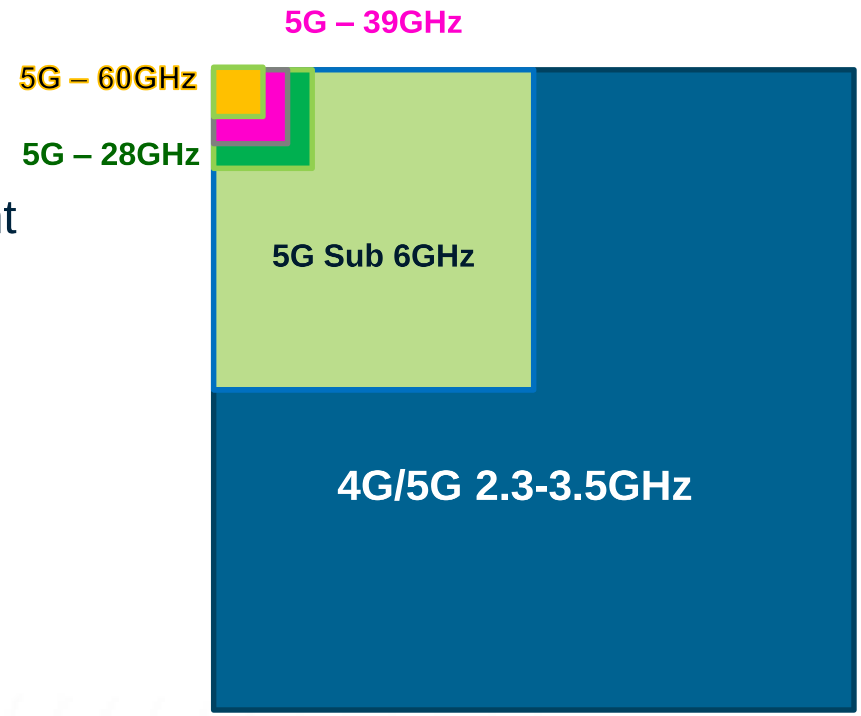
- Similar Concept To Phased Array Radar
- Enables Steerable Transmission Beams
- 2x2 to 8x8 Element Arrays
- Array Size Dictated by Radiating Element Spacing – λ/2
- Scales Directly with Frequency
  - 2.3 GHz – 6.5 cm } 4G
  - 3.5 GHz – 4.28 cm } 4G / Sub 6GHz 5G
  - 4.9 GHz – 3.06 cm } Sub 6GHz 5G
  - 28 GHz – 0.53 cm → mmW 5G
  - 39 GHz – 0.38 cm → mmW 5G
  - 60 GHz – 0.25 cm → mmW 5G
- Element Power Must Drop to Maintain Reasonable Array Temperatures
- Individual TR MMIC/Module Must Fit within the Horizontal Array Spacing
- MMIC Integration is Key - Esp mmW Solutions

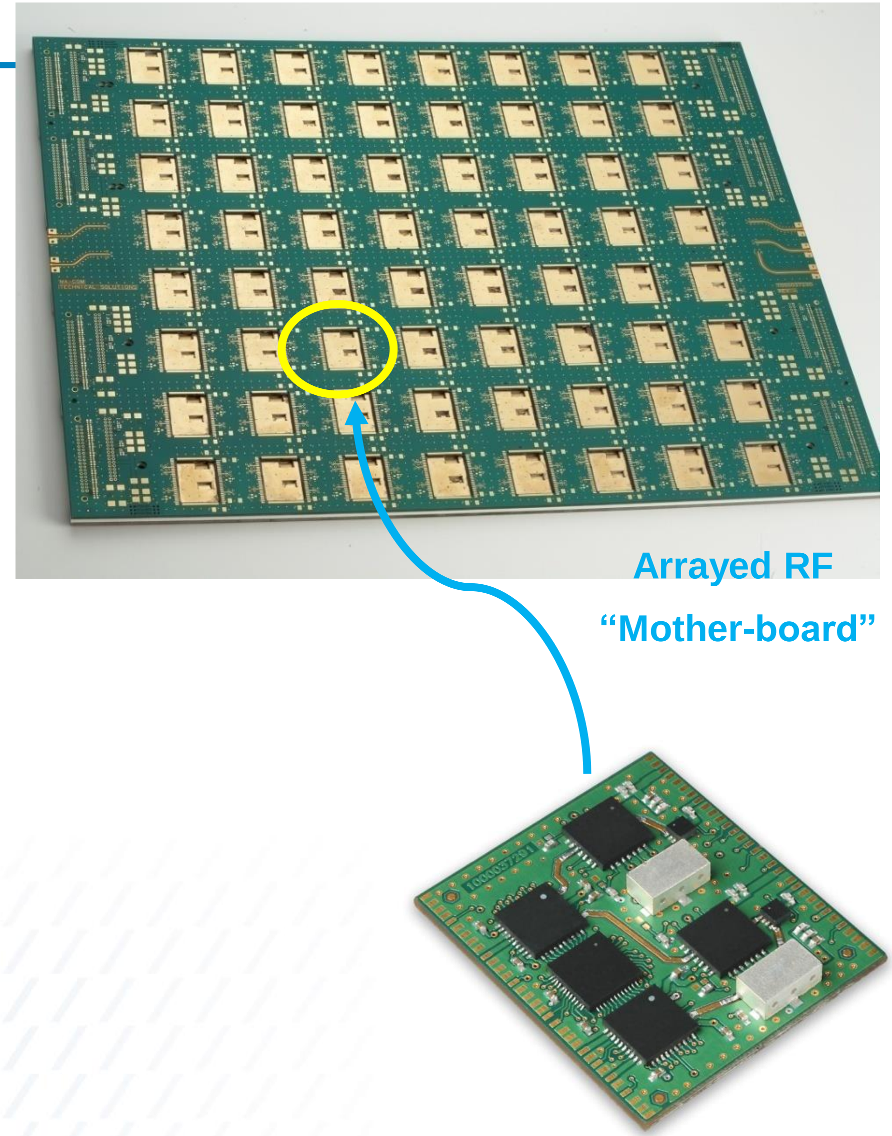


Relative Array Size for an NxN Planar Array

T/R Module

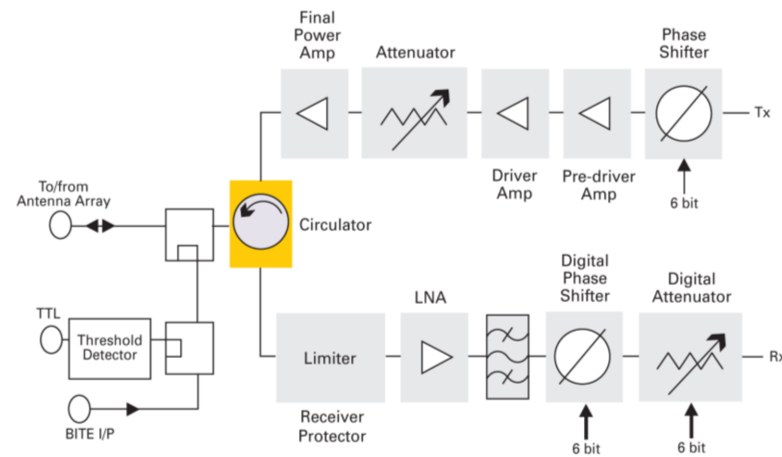
> Radiating Element Spacing
- $\lambda/2$
- S-Band => $\lambda/2 \approx$ 5 cm
- Relatively Large Array Spacing
  - Simplifies T/R Module Realization
  - Custom MMICs Individually Plastic Packaged
  - Modular PCB Integration

> T/R Module Concept
- Overall Dimensions - ≈ 3.0 cm x 3.5 cm
- Easily Fits into Required Array Spacing
- Land Grid Array
- Solder Tab I/O
- PCB - Five Layer Design
- Includes All DC, RF and Control Signal Routing
- Solder Reflow Insertion onto RF "Mother-board"
- Approach Applies Directly to Lower Frequencies



Why MMICs for mmW MIMO
Typical Transmit/Receive MMICs/Module

- **Transmit**
  - Phase Shifter
  - Pre-Driver/Driver Amplifier
  - Attenuator
- **HPA**
  - Final Transmit Power to Radiating Elements
- **Receive**
  - Phase Shifter
  - LNA
  - Limiter
  - Attenuator
  - Band Pass Filter
- **Common Leg Circuit Concepts**
  - Enables Phase Shifter/Attenuator to be Utilized in Both T_x and R_x
- **Isolation**
  - Circulator/High Power/Isolation Switch
  - SPDT Switch
- **Control Circuitry**
  - Digital Control in CMOS
  - Converts Serial Bit Stream for T_X and R_X Phase & Attenuation to Parallel Outputs
  - Control Capability to Determine Transmit State



Basic RF Transmit/Receive Module Block Diagram

GaN Revolution for 5G

GaN for 5G

- Only GaN-on-Silicon/GaN-on-Silicon MMICs at 5G Frequencies Can Meet ALL the Performance/Supply Chain Challenges
- Market vs Price
- GaN-on-Silicon vs GaN-on SiC
- New Rules/Challenges
- Supply Chain
- Future Expectations/Possibilities

The 5G GaN Revolution

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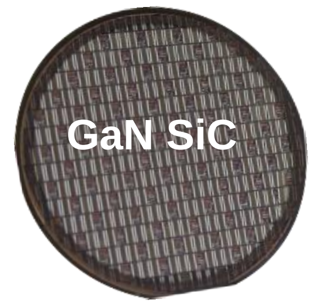
> Driving GaN to Mainstream Commercial Adoption

> GaN-on-SiC

- Small Diameters
- Small, Boutique FABs
- Limited Ability to Scale

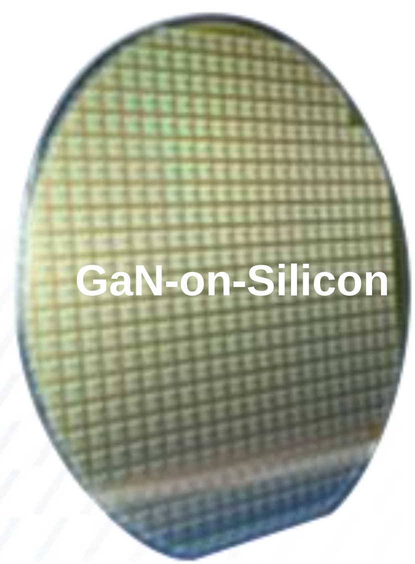
> GaN-on-Silicon

- Large Wafer Diameters
- Leverage High Volume Silicon
  - Processing Capability/Discipline
  - Supply Chain Robustness
  - Cost Structure
- Path to Full CMOS Silicon Integration



Defense Markets

Small Wafers – Small FABs



Global Commercial Markets

Large Wafers – High Volume FABs

GaN Must Compete on BOTH Cost and Performance to Win in the Market!!

GaN Performance at LDMOS Prices!!

Motivation for GaN-on-Silicon Industrialization

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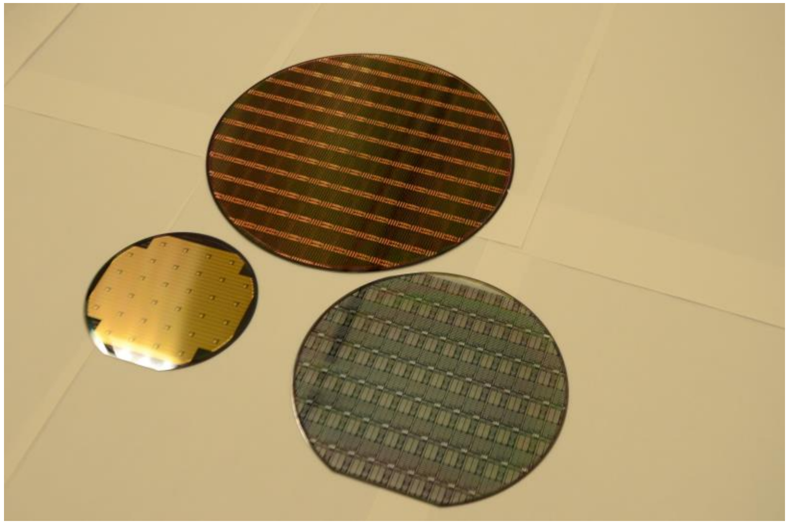
- **>** Market Opportunities – Everything Begins Here
- **>** Price Drives Volume – Volume Drives Cost
- **>** High Volume MOSFET Silicon Fab
- **>** Volume Capabilities of Typical CMOS Fab
  - Thousands of Wafers/Week
  - Wafer Diameter – 150mm (6”) -> 200mm (8”) -> 300mm (12”)
  - Cycle Times
    - Many Mask/Process Steps per Week
    - Provides Surge Capacity – Smooth Out Market Fluctuations
- **>** Price/Cost Drivers
  - GaN/Si – Existing Silicon Volume Spreads Overhead Costs
  - Large Wafer Diameters – 2.25x/4x/9x Increases in Die Count
  - High Line Yield



100mm – 150mm – 200mm GaN/Si Wafers

The Market Sets the Price

Market	Typical Device	Price Point
Aerospace and Defense	Broadband, High Efficiency, MMIC HPA • 10 – 1000 W • 28/48 V operation	$2.00 – $5.00/Watt
CATV	Low Frequency, Broadband, High Linearity	$0.5 – $1.00
Infrastructure	Discrete Power Transistors	$0.15 – $0.30/Watt

- The lowest cost solution ***always*** wins in the marketplace
- So …. If Silicon can do …. Silicon will win ….
- So …. If Silicon can't & GaAs can …. GaAs will win ….
- GaN needs to provide unique solutions & provide compelling value to win

Silicon vs. SiC Wafer Substrate Production

Silicon Ingot

(6” wafer = $20)

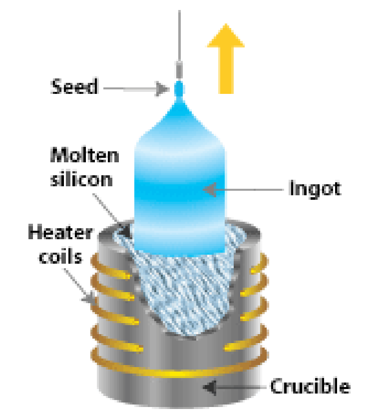


Illustration courtesy of EERE & U.S. Dept. of Energy

Silicon Ingot Pulling

≈1400 ° C

>3 inches/hr

SiC Ingot (6” wafer = $6000)

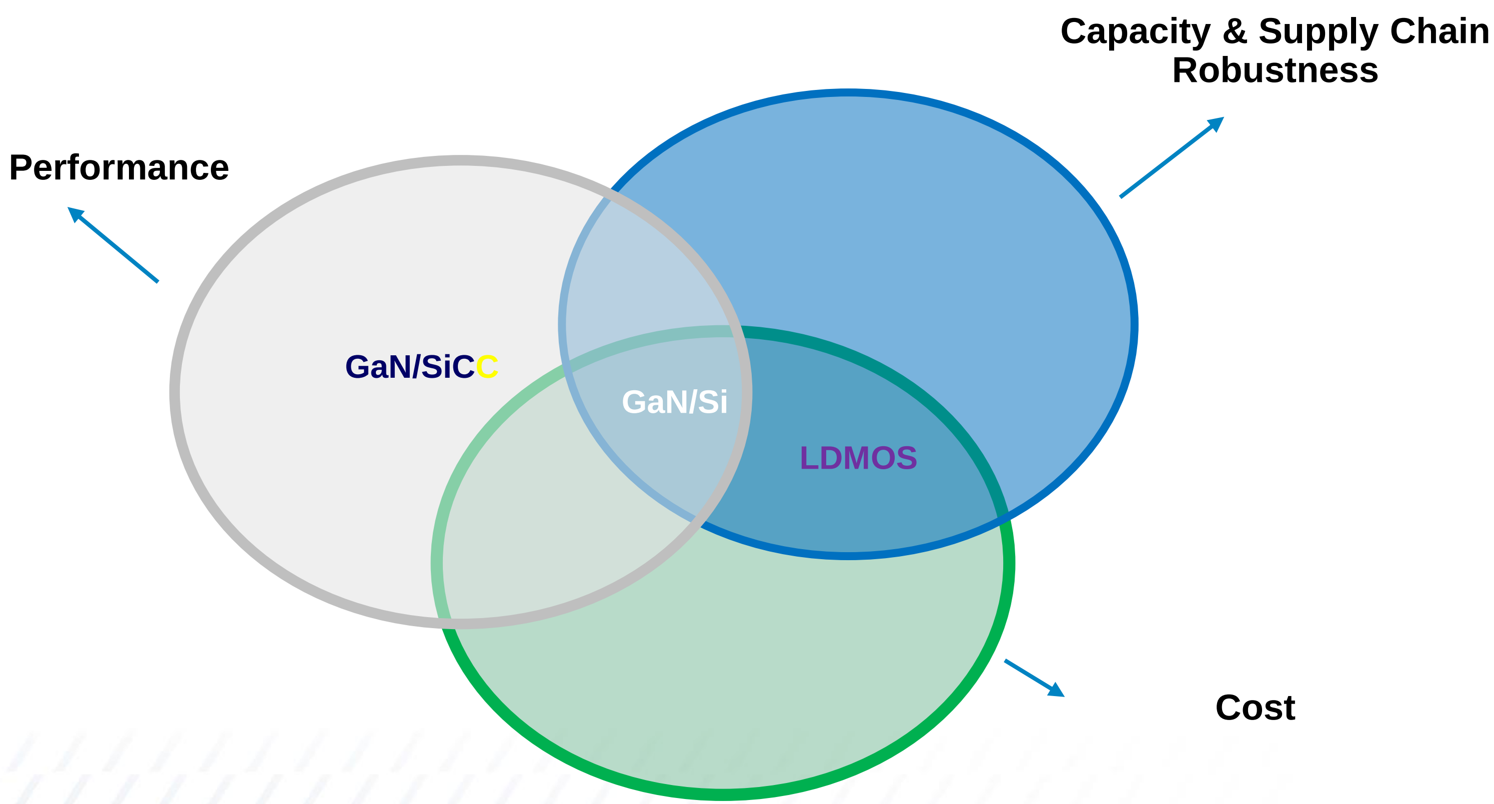
High Temperature (>2000ºC)

PVT SiC Ingot Growth Reactor

100µm/hr - 200µm/hr

3000 Si wafers from a single ingot vs. < 100 SiC wafers from a SiC “ingot”

GaN/Si Positioning

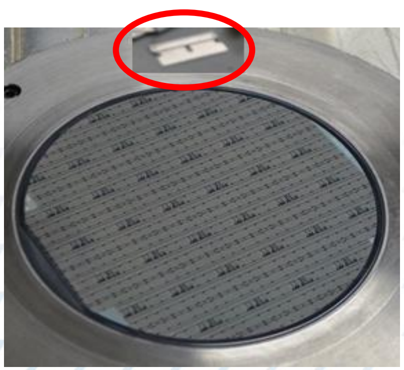


GaN/Si

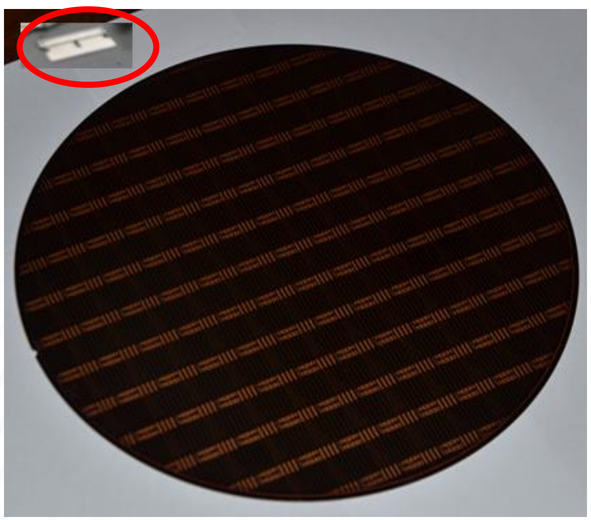
Offers the Best of All Requirements
Performance
Cost
Scalability
Supply Chain Robustness

GaN Future Directions

- Happening NOW!!
- GaN-on-Silicon - Integrated in Large Diameter, High Volume, Silicon Fab
  - Needs “Large” Silicon Fab Partners
  - “Large” = 150mm/200mm Diameter 3000 – 15,000 wfs/wk
- Process Must Adapt
  - Gold Free Processing – Aluminum/Copper Based Metallization
  - Dielectric Crossovers
  - Deep UV Steppers
  - Hands Off, Cassette-to-Cassette Processing
  - NO Recycles – Process Must Work First Time/Every Time



150 mm (6 inch) GaN/Si wafer (Power MOS Fab) with HF/RF/μW HEMT Devices

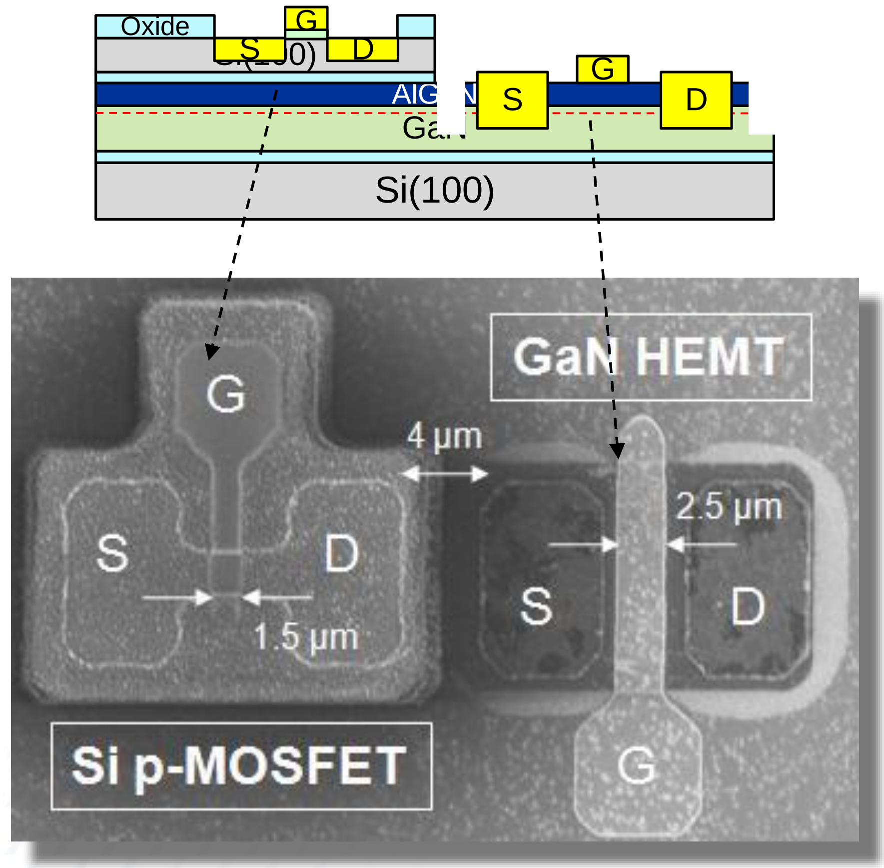


200 mm (8 inch) GaN/Si wafer (CMOS Fab) with HF/RF HEMT Devices

GaN Future Directions

> GaN/MOSFET Integration

- Integration of III-V HEMTs and Si (100) MOSFETs
- High power digital-to-analog converters (DACs)
- On-wafer wireless transmitters
- Driver stages for on-wafer optoelectronics
- Power amplifiers coupled to Si linearizer circuits
- High speed (high power) differential amplifiers
- Normally-off power transistors
- New enhancement-mode power transistors
- Buffer stages for ultra-low-power electronics



Conclusions

Silicon is the MOST Mature, Defect-Free, Lowest Cost Substrate for Solid State Applications

Only GaN/Si can be Scaled to ≥200mm Wafer Fabs & Meet the Volume Ramp Requirements for BTS and RFE Market Adoption

GaN/Si A&D Devices have Demonstrated Similar/Superior Performance to Equivalent GaN/SiC Devices

GaN/Si RFE Devices have Demonstrated Superior Efficiency, PAE Flatness, with Virtually Identical Output Power and Gain to LDMOS devices

GaN/Si Uniquely Enables Homogeneous Integration with CMOS

GaN/Si is Ideally Suited to Service Volume/Basestation RF Markets